**Practitioner's Docket No. 13189.144**

**CHAPTER II**

Preliminary Classification:
Proposed Class: Unknown
Subclass: Unknown

**TRANSMITTAL LETTER**
**TO THE UNITED STATES ELECTED OFFICE (EO/US)**
**(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)**

| PCT/EP00/05772 | 21 June 2000 (21.06.00) | 1 July 1999 (01.07.99) |
|---|---|---|
| **International Application Number** | **International Filing Date** | **International Earliest Priority Date** |

TITLE OF INVENTION: METHOD OF SUBDIVIDING A WAFER
APPLICANT(S): Feil, Michael; Landesberger, Cristof; Klumpp, Armin; and Hacker, Erwin

**ATTENTION: EO/US**
**Box PCT**
**Assistant Commissioner for Patents**
**Washington DC 20231**

1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. Section 371:

   a. This express request to immediately begin national examination procedures (35 U.S.C. Section 371(f)).
   b. The U.S. National Fee (35 U.S.C. Section 371(c)(1)) and other fees (37 C.F.R. Section 1.492) as indicated below:

**CERTIFICATION UNDER 37 C.F.R. SECTION 1.10***
*(Express Mail label number is **mandatory.**)*
*(Express Mail certification is optional.)*

I hereby certify that this paper, along with any document referred to, is being deposited with the United States Postal Service on this date 12/19/01 in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EV011000222US addressed to ATTENTION. EO/US, Box PCT, Assistant Commissioner for Patents, Washington, DC 20231

Cheryl Martinez
*(type or print name of person mailing paper)*

**Signature of person mailing paper**

Doc. 3874

2. Fees

| CLAIMS FEE* | (1) FOR | (2) NUMBER FILED | (3) NUMBER EXTRA | (4) RATE | (5) CALCULATIONS |
|---|---|---|---|---|---|
| | TOTAL CLAIMS | 8 -20 = | 0 | x $18 00 = | $0 00 |
| | INDEPENDENT CLAIMS | 1 - 3 = | 0 | x $84.00 = | $0.00 |
| | MULTIPLE DEPENDENT CLAIM(S) (if applicable) + $280.00 | | | | $0.00 |
| BASIC FEE | U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in Section 1.482 has been paid to the U.S. PTO, and payment of an international search fee as set forth in Section 1.445(a)(2) to the U S. PTO: where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 C.F.R. Section 1.492(a)(5)) ..... $890.00 | | | | $890.00 |
| | Total of above Calculations | | | | = $890 00 |
| SMALL ENTITY | Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed. (note 37 CFR Sections 1.9, 1.27, 1.28) | | | | - $0.00 |
| | Subtotal | | | | $890 00 |
| | Total National Fee | | | | $890.00 |
| TOTAL | Total Fees enclosed | | | | $890.00 |

Please charge Account No. 50-1848 in the amount of $890.00. A duplicate copy of this sheet is enclosed.

3. A copy of the International Application as filed (35 U.S.C. Section 371(c)(2)) is transmitted herewith.

4. A translation of the International Application into the English language (35 U.S.C. Section 371(c)(2)) is transmitted herewith.

5. Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. Section 371(c)(3)) have not been transmitted. Applicant chose not to make amendments under PCT Article 19 or Article 34.

Date of mailing of Search Report (from form PCT/ISA/220): November 21, 2000

6. A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. Section 371(c)(3)) has not been transmitted for reasons indicated in Section 5.

7. A copy of the International Preliminary Examination Report (PCT/IPEA/416) is transmitted herewith.

8. Annexes to the International Preliminary Examination Report are transmitted herewith.

9. A translation of the annexes to the International Preliminary Examination Report is transmitted herewith.

10. An oath or declaration of the inventor (35 U.S.C. Section 371(c)(4)) complying with 35 U.S.C. Section 115 will follow.

11. An Information Disclosure Statement under 37 C.F.R. Sections 1.97 and 1.98 will be transmitted within three (3) months of filing this application.

II. Other document(s) or information included:

12. An International Search Report (PCT/ISA/220) or Declaration under PCT Article 17(2)(a) is transmitted herewith.

13. Additional documents:

a. International Publication No. WO 01/03180 (front page only)
b. Preliminary Amendment (37 C.F.R. Section 1.121)
c. Final version of PCT/EP00/05772 for the prosecution at the USPTO to be filed as first preliminary amendment
d. Annotated copy of Final version of PCT/EP00/05772
e. Drawings
f. Express Mail Certificate
g. Return Postcard

14. The above items are being transmitted before 30 months from any claimed priority date.

**AUTHORIZATION TO CHARGE ADDITIONAL FEES**

The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No. 50-1848:

37 C.F.R. Section 1.492(a)(1), (2), (3), and (4) (filing fees)
37 C.F.R. Section 1.492(b), (c), and (d) (presentation of extra claims)
37 C.F.R. Section 1.17 (application processing fees)
37 C.F.R. Section 1.17(a)(1)-(5) (extension fees pursuant to Section 1.136(a))
37 C.F.R. Section 1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 20 months after the priority date).

Date: 12/18/01

Signature of Practitioner

Reg. No.: 28,494
Tel. No.: 303-379-1114

Carl A. Forest
**Customer No.: 24283**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**AS DESIGNATED/ELECTED OFFICE DO/EO/US**

U.S. Patent Application No.: Applied For
International Application No.: PCT/EP00/05772
International Filing Date: 21 June 2000
Priority Date: 1 July 1999
For: Method Of Subdividing A Wafer
Applicants (Inventors):
Feil et al.

Group Art Unit: Unknown
Examiner: Unknown
Docket No: 13189.144

ATTENTION: EO/US
BOX PCT
ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, DC 20231

December 18, 2001

Dear Sir:

**FIRST PRELIMINARY AMENDMENT**

In the Specification:

Please substitute the attached specification entitled "Final version of PCT/EP00/05772 for the prosecution at the USPTO to be filed as first preliminary amendment" for the original PCT specification.

In the Claims:

Please substitute the enclosed claims 1 - 8, on pages 14 – 16, inclusive, attached to the substitute specification, for original claims 1 - 8.

In the Abstract:

Please substitute the enclosed abstract, attached to the substitute specification on page 17 for the original abstract.

**REMARKS**

Applicants respectfully request that the Examiner base the examination upon the attached substitute specification, claims, and abstract. An Annotated Copy Of Final Version Of PCT/EP00/05772 is enclosed showing the revisions made in the substitute specification, claims, and abstract.

The PCT specification, claims, and abstract have been revised to conform to U.S. requirements. It is believed that no new matter was introduced in revising the specification, claims, and abstract.

In view of the foregoing amendments, it is believed that the application, including claims 1 – 8, is in condition for allowance, and favorable action is respectfully requested. The Examiner is invited to contact the undersigned by collect telephone call to advance the prosecution in any respect.

No additional fee for this Preliminary Amendment is seen to be required. If any additional fee is required, please charge it to Deposit Account No. 50-1848.

Respectfully submitted,
**PATTON BOGGS LLP**

By: _____

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National Phase of PCT/EP00/05772 in U.S.A.
Title: Method of Subdividing a Wafer
Applicants: FEIL, Michael et al.

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**Final version of PCT/EP00/05772 for the prosecution at the USPTO to be filed as first preliminary amendment**

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# Method of Subdividing a Wafer

## Description

The present invention relates to the production of integrated circuits and, in particular, to a method of dicing a wafer, which comprises a plurality of individual circuit structures, so as to obtain very thin circuit chips.

Recently, there has been an increasing demand for thin chips on the one hand and high flexibility on the other so as to be able to use electronic circuit chips in a great variety of cases. The demand for thin circuit chips results, on the one hand, from increasingly complex electronic systems which should be composed of individual, fully processed chips that can be obtained from various manufacturers; simultaneously, these electronic systems should also be suitable for use in the field of high-frequency technology and they should take up little space. In order to keep the price of the whole system low, it should be possible to build up such chips, or modules including such chips, by means of conventional, economy-priced manufacturing methods.

One of the essential demands is, in particular, that pre-processed chips, which can be acquired as finished components, should be usable for the greatest possible number of applications so as to be e.g. independent of a single chip manufacturer, or so as to avoid the necessity of developing one's own chips, which would lead to higher prices in many cases, and so as to be able to concentrate exclusively on the interconnection of the individual chip components when a new system is being developed. Investigations have shown that e.g. in the case of simple silicon circuit chips up to 90 % of the added value of the

future product lie in the sphere of assembly and connection technologies, but not in the manufacture of the wafer from which the individual circuit chips can be produced by dicing.

It follows that pre-processed wafers must be used for obtaining the individual circuit chips by dicing.

US patent No. 4,722130 describes a method of producing semiconductor chips by dicing a semiconductor wafer. For this purpose, the front of the wafer has formed therein a lattice-shaped trench, whereupon an adhesive nylon foil, which is adherent on one side, is applied to the wafer front having the trench formed therein. Subsequently, the back of the support is ground so as to thin the wafer down to a defined thickness, the thickness of the thinned wafer being chosen such that the individual circuit chips, which have already been defined by the trenches, are interconnected by comparatively thin connection bridges. For separating the individual circuit chips, which are connected by connection bridges, the adhesive nylon foil is stripped off from one side of the wafer; this has effect that the connection bridges between the circuit chips break due to the pulling effect occurring when the adhesive foil is being stripped off. When the adhesive foil has been stripped off, the diced chips are still attached to an elastic support foil on the opposite side of the chip, which has been attached prior to stripping off the adhesive nylon foil. The elastic adhesive foil is then stretched transversally, whereby the spaces between the circuit chips are widened; this is easily possible, since the connection bridges have already been broken. The individual circuit chips can then be removed and inserted or used where they are needed. Circuit chips produced in this way have a thickness of approx. 160 µm; the starting material used was a standard GaAs wafer

which had a thickness of 630 µm before it was thinned by grinding.

This method is disadvantageous insofar as it cannot be used for producing very thin and, consequently, also very sensitive chips. The mechanical thinning and the mechanical dicing of the chips by breaking the connection bridges entails the danger that the individual chips may be mechanically damaged or may have rough or even torn edges. In the case of chips having a thickness of 160 µm, such problems are not yet very grave. If the chips to be produced are, however, chips having a thickness of less than 50 µm, and, in particular, less than 20 µm, such tears may cause high production losses due to the mechanical processing of the back and the mechanical breaking of the connection bridges, since, due to the very small thickness, it may easily happen that active regions of the chips are impaired or even destroyed.

It is the object of the present invention to provide a reasonably-priced but still reliable method of dicing a wafer for obtaining very thin circuit chips.

This object is achieved by a method according to claim 1.

The present invention is based on the finding that, for obtaining very thin circuit chips, mechanical effects must be eliminated as far as possible when the wafer is being diced. The danger that individual circuit chips may be damaged due to mechanical effects can be reduced markedly in this way. When very thin circuit chips are produced, it must be taken into account that the active region of a circuit chip may extend as deep as a few micrometers into the semiconductor material. When thin circuit chips having a thickness in the order of 20 µm are considered,

**Amended Sheets (pages 3a and 3b)**

WO 99/25019 refers to a method of thinning semiconductor wafers. In a first step, a plurality of grooves is defined in the front of a semiconductor wafer. The grooves separate each integrated circuit such that it defines a separate chip. The grooves extend only partially into the front. When the grooves have been produced, a polyimide layer is applied so as to planarize the wafer provided with the grooves, the polyimide layer being used as a stress compensation layer for the subsequent thinning operation executed by means of grinding. This polyimide layer has applied thereto an adhesive layer by means of spraying or spinning. The wafer is then placed on a surface of a substrate in such a way that the adhesive layer faces said surface. In order to fix the wafer to the substrate, a predetermined pressure and a predetermined temperature are used so as to cure the adhesive layer. Following this, the wafer is thinned from the back by means of grinding. The thinned wafer is then placed on a needle block and immersed in a solvent so as to dissolve the adhesive layer; making use of a vacuum device, the individual chips are then removed from the needle block and placed in chip carriers.

US-pat. 5,071,792 refers to a method of forming ultrathin integrated circuit chips. In a first step, grooves are produced in the front of the wafer. These grooves are then filled with a hard material acting as a grinding stop. This material is then planarized and a wax is applied thereto, which provides a temporary adhesion between a passivation coating and the planar surface of an intermediate support. Following this, the back of the wafer is ground so as to dice the chips. The comparatively hard material in the grooves acts here as a grinding stop. After the grinding process, the grinding stop material is removed from the

grooves. In order to obtain the individual chips, the wax film is finally melted.

It is the object of the present invention .....

Amended sheet

only less than 20 µm will remain as a "support substrate" for the active region of the circuit chip. The present invention therefore departs from the concept of mechanical dicing, which is accomplished e.g. by scribing, sawing or breaking of thin connections defined by trenches, as has been explained hereinbefore, an executes dicing by means of dry etching from the back.

According to the present invention, a wafer comprising a plurality of circuit structures is diced in such a way that a trench is first defined between at least two circuit structures. Subsequently, the trench is deepened down to a defined depth. Following this, a re-detachable intermediate support is fixed to the wafer face having the trench formed therein, whereupon the wafer is subjected to dry-etching from the opposite face until the trenches are exposed. In this way, a dicing process is achieved in the case of which the circuit chips have not been subjected to mechanical stresses.

When, in accordance with a specially preferred embodiment, also the trench is formed by dry-etching instead of being formed mechanically, the individual circuit chips will not be subjected to any mechanical stress at all during the whole wafer dicing process. This has the effect that also very thin circuit chips can be produced, without any marked increase in the reject rate.

According to a preferred embodiment, the wafer is pre-thinned by means of wet-chemical etching or grinding before the back is subjected to dry-etching, the pre-thinning with the aid of mechanical means being executed only to such an extent that it is almost impossible that the material which will finally form the circuit chips has already been impaired mechanically.

The component used as an intermediate support is preferably an adhesive foil which is adherent on both sides and one side of which adheres to a wafer substrate, whereas the other side thereof is connected to the wafer to be diced and has a variable adhesive strength so that, after the dry-etching step, the adhesive strength of this side of the adhesive foil can be reduced to such an extent that the diced circuit chips can easily be detached for further processing, said reduction of the adhesive strength being caused by heating or by exposure to UV radiation.

Even if the trench is implemented by means of careful mechanical processing methods, it will already be possible to produce a plurality of circuit chips with a comparatively low reject rate due to the dry-etching from the back for the purpose of dicing the wafer. Such circuit chips can have a thickness which is less than 50 µm and which especially amounts to about 20 µm and can even be reduced down to 5 µm.

If, however, in accordance with the preferred course of action, also the trench is produced by dry-etching, i.e. without subjecting the material to excessive stress, a certain number of further advantages will be achieved insofar as the wafer areas which will finally define the thin circuit chips are not subjected to any mechanical stresses at all.

Due to the fact that the trench need not be particularly deep, since the chips are very thin, the formation of a trench in a process making use of a mask for etching is, in general, carried out in a comparatively short period of time so that, in comparison with sawing of a wafer, which may last several hours especially in the case of small chips and wafers having a diameter of 20 to 30 cm, a substantial increase in the throughput can be achieved. In addition, a substantially larger number of chips

can - again in comparison with sawing - be accommodated on a wafer, especially in the case of small chips, since trenches produced by sawing normally have a thickness of approx. 100 µm, whereas only 10 µm will suffice for dry-etched trenches down to the aimed-at depth, which will correspond approximately to the thickness of the circuit chips. In particular in the case of small chips, the number of chips per wafer can be increased by up to 10 to 15%.

Due to the fact that at least the back of the chips and, preferably, also the lateral edges thereof are subjected to an etch treatment, the chips are mechanically undamaged; this will be particularly important when the chips have to be bent, as will e.g. the case if the chips have to be incorporated in electronic labels.

Finally, arbitrary chip shapes can be produced especially by dry-etching the trench, i.e. the chip shapes that can be produced are not limited to rectangular shapes, as in the case of sawing; this can be of decisive importance especially in connection with power semiconductors, since chip corners, which would otherwise generate very high electric fields, can be eliminated. Finally, also the position of the chips can unequivocally be identified from the back, a circumstance which will be of great advantage e.g. for die bonding and for recognizing chips of good quality and those of poor quality.

In the following, preferred embodiments of the present invention will be explained in detail making reference to the drawings enclosed, in which:

Fig. 1 shows a top view of a wafer which comprises a plurality of circuit chips and in which a trench is defined;

Fig. 2 shows a cross-sectional view of the wafer of Fig. 1 having the trench formed therein;

Fig. 3 shows a view of the wafer of Fig. 2 which is secured to an intermediate support;

Fig. 4 shows a view of the wafer of Fig. 3 after thinning of the wafer by means of a dry-etching process; and

Fig. 5 shows the individual circuit chips after their removal from the intermediate support.

Fig. 1 shows a top view of a detail of a wafer 10 comprising a plurality of fully processed individual circuit structures 12a, 12b. The wafer 10 has already defined thereon a trench 14. In cases in which the trench 14 is produced mechanically, the trench can be defined e.g. by inputting the coordinates for a sawing or scribing means. In cases in which the trench 14 is produced by making use of a dry-etching process, the trench is formed by applying a resist mask with side-wall protection by polymer deposition. Alternatively, the etch mask defining the trench 14 can also be implemented as an $SiO_2$ mask. Summarizing, it can be stated that all the methods of forming an etch mask can be used for defining the trench 14.

Fig. 2 shows a cross-sectional view along the line A-A of Fig. 1 through the wafer 10 in a state in which the trench 14 has been formed down to a certain depth d. The predetermined thickness is chosen such that it is at least equal to the target thickness of the circuit chip to be produced so that the circuit chips can be diced later on without being mechanically acted upon.

If e.g. the process with polymer deposition is used, $SF_6$ can be used as an etching gas and $CHF_3$ and $C_2F_6$ can be used as polymer protection. More details with regard to this method are disclosed in DE 4241045.

If a process with an $SiO_2$ mask is used, a mixture of HBr, $Cl_2$, $O_2$ and He can be used as an etching gas. In addition, all the other known dry-etching processes can be used. Dry-etching in general has the substantial advantage that, in contrast to a mechanical implementation of the trench, the edges of the circuit chip are not subjected to mechanical stress and are therefore stable.

Fig. 3 shows the circuit chip 10, which is provided with the trench 14, after it has been secured to an intermediate support which can be composed of a substrate wafer 16a and an adhesive medium 16b. The medium used as an adhesive medium 16b is preferably an adhesive foil which is adherent on both sides, one side of this adhesive foil being provided with a special coating which loses its adhesive strength when it has been heated to a temperature of e.g. 90 to 140°. The other side does not have a varying adhesive strength. The support foil is attached in such a way that the side with the non-varying adhesive strength is connected to the wafer support 16a, whereas the side with the varying adhesive strength is connected to the semiconductor wafer 10, as can be seen in Fig. 3. An essential property of the intermediate support 16a, 16b is that the adhesive connection with the wafer 10 can be released. In addition, a full-area, cavity-free connection will be of advantage.

Alternative materials for the adhesive medium 16b are thermoplastic materials or adhesive foils whose adhesive strength can be varied not by means of heat but by means of UV light. If UV-sensitive foils are used, the support substrate 16a must be

transparent. In this case, a glass wafer can be used as a support substrate.

When the wafer 10 has been glued onto the intermediate support 16a, 16b, the wafer is thinned from the back, as shown in Fig. 4. If the initial wafer 10 is already comparatively thin, it will presumably suffice to use only a dry-etching process so as to separate the individual circuit chips from one another, i.e. so as to remove the back at least up to the trench. If the wafer in question is, however, a thick wafer, e.g. a wafer having a thickness of 700 µm, which is a typical value for commercially available wafers, a faster method, such as mechanical grinding, wet etching or the like, is preferably used prior to the final dry-etching step for dicing the circuit chips. A method which proved to be advantageous is the so-called spin-etching in the case of which the wafer lies on a rotating disk while the etching medium flows onto the disk from above and is spun off therefrom.

When the wafer has been pre-thinned to a predetermined thickness, the last step of dicing is left to the dry-etching process. The etching gases preferably used for executing this step are the etching gas mixture $Cl_2$ and $CF_4$, or $SF_6$ as a single etching gas. It should here be noted that a chemical treatment with chlorine and fluorine is generally well suited for etching silicon. The etching gas $NF_3$ is very efficient as well, but, at present, it is still comparatively expensive; hence, it is one of the less preferred etching gases at the present time.

As can be seen in Fig. 4, individual circuit chips 18, 20, 22 and 24 have now been created, which are no longer connected to one another but which are only held by the adhesive medium 16b. In cases in which an adhesive foil is used which is adherent on

both sides and which has a variable adhesive strength on one side thereof, the individual circuit chips 18, 20, 22, 24 can now easily be removed by varying the adhesive strength so that they will then exist completely independently of one another, as can be seen in Fig. 5, whereupon they are picked up by an assembly machine or a similar device so as to be accommodated at their final location.

It should here be pointed out that this method is suitable not only for silicon wafers but also for GaAs wafers, which are particularly sensitive to mechanical stress due to their brittleness, as well as for other III-V semiconductors. It goes without saying that for semiconductor materials other than silicon etching gases other than the above-mentioned ones are also used.

The diced thin circuit chips 18, 20, 22, 24 can be used in electronic components and systems requiring an extremely small volume demand, e.g. in mobile telecommunications systems or medical monitoring and assistance systems, such as hearing aids, cardiac pacemakers, monitoring and diagnostic units worn on the body, etc..

Other fields of use are electronic components which are optimized for electric signal transmission, such as high-frequency components.

Finally, the thin circuit chips diced according to the present invention can be combined so as to obtain circuit modules which comprise individual components consisting of different basic materials or in which chips originating from different manufacturing technologies are joined. Ultrathin circuit chips can be used especially in systems consisting of memory chips, logic chips,

sensor components, chip-card chips, power components or high-frequency transmission chips (transponders).

Due to their very small thickness, thin circuit chips produced according to the present invention contribute to the overall volume of the component only as a thin film. A complete chip system consisting e.g. of a normal chip and an ultrathin chip is, in the final analysis, not much larger than a standard integrated circuit.

Due to the small thickness of the diced circuit chips, it is now also possible to use surface treatment techniques for contacting and wiring individual chips in a multi-chip module making use of conventional techniques which require planar or almost planar surfaces.

Finally, the method according to the present invention can be used for dicing not only specially produced or pretreated circuit wafers but all wafers which can be obtained from arbitrary manufacturers as fully processed wafers.

**Amended Claims**

Claims

1. A method of dicing a wafer (10) which comprises a plurality of circuit structures (12a, 12b), said method comprising the steps of:

defining a trench (14) between at least two circuit structures (12a, 12b) on one face of the wafer (10);

forming the trench (14) down to a defined depth (d) by means of dry etching;

fixing to said one face of the wafer (10) a re-detachable intermediate support (16a, 16b) composed of a fixed intermediate support substrate (16a) and an adhesive medium (16b) which is applied to said intermediate support substrate and which can specifically be modified in terms of its adhesive strength, said adhesive medium (16b) being an adhesive foil which is adherent on both sides, the side of the adhesive foil which is secured to said one face of the wafer having the variable adhesive strength, and said adhesive strength being adapted to be reduced by heating;

thinning the wafer, which is secured to the intermediate support (16a, 16b), from the opposite face by means of dry etching so as to obtain individual circuit chips (18, 20, 22, 24) which are held by the intermediate support (16a, 16b); and

removing the individual circuit chips (18, 20, 22, 24) from the intermediate support (16a, 16b) by heating said intermedi-

Amended sheet

ate support (16a, 16b) so as to reduce the adhesive strength of said adhesive foil (16b) to such an extent that the circuit chips (18, 20, 22, 24) can be detached from the intermediate support.

2. A method according to claim 1, wherein the dry-etching step of the other face of the wafer (10) is executed until the circuit chips have a thickness which is smaller than 50 µm and which is preferably 20 µm.

3. A method according to claim 1,

wherein the forming of the trench is carried out such that a predetermined thickness is reached, which corresponds to a target chip thickness; and

wherein the step of dry-etching the other face of the wafer is executed until the trench has substantially been reached.

4. A method according to one of the preceding claims,

wherein, prior to the step of dry etching the other face of the wafer (10), a pre-thinning step is executed in such a way that the circuit chips are still interconnected across the trench (14) and that the thickness of this connection has a specific value.

5. A method according to claim 4, wherein the pre-thinning step comprises grinding, wet-chemical etching or a combination thereof.

6. A method according to one of the claims 1 to 5, wherein in the trench-defining step a trench having at least one round por-

tion is defined.

7. A method according to one of the preceding claims, wherein the wafer consists of Si, GaAs or some other III-V semiconductor.

8. A method according to one of the claims 1 to 7, wherein the defining step comprises the application of an $SiO_2$ mask or of a resist mask with side-wall protection by polymer deposition.

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**Method of Subdividing a Wafer**

Abstract

In a method of dicing a wafer (10), which comprises a plurality of individual circuit structures (12a, 12b), a trench (14) is first defined between at least two circuit structures (12a, 12b) on one face of the wafer. Subsequently, the trench is deepened down to a defined depth. Following this, one face of the wafer has fixed thereto a re-detachable intermediate support composed of a fixed intermediate support substrate and an adhesive medium which is applied to said intermediate support substrate and which can specifically be modified in terms of its adhesive strength, whereupon the wafer is dry-etched from the opposite face so that circuit chips are obtained which are connected to one another only via the intermediate support. Subsequently, the circuit chips are removed from the intermediate support. This method substantially reduces mechanical impairments that may occur during dicing of the circuit chips; on the one hand, this permits the production of circuit chips with a thickness of less than 50 µm and, on the other hand, it leads to mechanically substantially undamaged circuit chips.

National Phase of PCT/EP00/05772 in U.S.A.
Title: Method of Subdividing a Wafer
Applicant: FEIL, Michael et al.

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**Translation of PCT Application PCT/EP00/05772**
**as originally filed**

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# Method of Subdividing a Wafer

## Field of the Invention

The present invention relates to the production of integrated circuits and, in particular, to a method of dicing a wafer, which comprises a plurality of individual circuit structures, so as to obtain very thin circuit chips.

## Background of the Invention and Prior Art

Recently, there has been an increasing demand for thin chips on the one hand and high flexibility on the other so as to be able to use electronic circuit chips in a great variety of cases. The demand for thin circuit chips results, on the one hand, from increasingly complex electronic systems which should be composed of individual, fully processed chips that can be obtained from various manufacturers; simultaneously, these electronic systems should also be suitable for use in the field of high-frequency technology and they should take up little space. In order to keep the price of the whole system low, it should be possible to build up such chips, or modules including such chips, by means of conventional, economy-priced manufacturing methods.

One of the essential demands is, in particular, that pre-processed chips, which can be acquired as finished components, should be usable for the greatest possible number of applications so as to be e.g. independent of a single chip manufacturer, or so as to avoid the necessity of developing one's own chips, which would lead to higher prices in many cases, and so as to be able to concentrate exclusively on the interconnection

of the individual chip components when a new system is being developed. Investigations have shown that e.g. in the case of simple silicon circuit chips up to 90 % of the added value of the future product lie in the sphere of assembly and connection technologies, but not in the manufacture of the wafer from which the individual circuit chips can be produced by dicing.

It follows that pre-processed wafers must be used for obtaining the individual circuit chips by dicing.

US patent No. 4,722130 describes a method of producing semiconductor chips by dicing a semiconductor wafer. For this purpose, the front of the wafer has formed therein a lattice-shaped trench, whereupon an adhesive nylon foil, which is adherent on one side, is applied to the wafer front having the trench formed therein. Subsequently, the back of the support is ground so as to thin the wafer down to a defined thickness, the thickness of the thinned wafer being chosen such that the individual circuit chips, which have already been defined by the trenches, are interconnected by comparatively thin connection bridges. For separating the individual circuit chips, which are connected by connection bridges, the adhesive nylon foil is stripped off from one side of the wafer; this has effect that the connection bridges between the circuit chips break due to the pulling effect occurring when the adhesive foil is being stripped off. When the adhesive foil has been stripped off, the diced chips are still attached to an elastic support foil on the opposite side of the chip, which has been attached prior to stripping off the adhesive nylon foil. The elastic adhesive foil is then stretched transversally, whereby the spaces between the circuit chips are widened; this is easily possible, since the connection bridges have already been broken. The individual circuit chips can then be removed and inserted or used where they are needed.

Circuit chips produced in this way have a thickness of approx. 160 µm; the starting material used was a standard GaAs wafer which had a thickness of 630 µm before it was thinned by grinding.

This method is disadvantageous insofar as it cannot be used for producing very thin and, consequently, also very sensitive chips. The mechanical thinning and the mechanical dicing of the chips by breaking the connection bridges entails the danger that the individual chips may be mechanically damaged or may have rough or even torn edges. In the case of chips having a thickness of 160 µm, such problems are not yet very grave. If the chips to be produced are, however, chips having a thickness of less than 50 µm, and, in particular, less than 20 µm, such tears may cause high production losses due to the mechanical processing of the back and the mechanical breaking of the connection bridges, since, due to the very small thickness, it may easily happen that active regions of the chips are impaired or even destroyed.

WO 99/25019 refers to a method of thinning semiconductor wafers. In a first step, a plurality of grooves is defined in the front of a semiconductor wafer. The grooves separate each integrated circuit such that it defines a separate chip. The grooves extend only partially into the front. When the grooves have been produced, a polyimide layer is applied so as to planarize the wafer provided with the grooves, the polyimide layer being used as a stress compensation layer for the subsequent thinning operation executed by means of grinding. This polyimide layer has applied thereto an adhesive layer by means of spraying or spinning. The wafer is then placed on a surface of a substrate in such a way that the adhesive layer faces said surface. In order to fix the wafer to the substrate, a predetermined pressure and a predeter-

mined temperature are used so as to cure the adhesive layer. Following this, the wafer is thinned from the back by means of grinding. The thinned wafer is then placed on a needle block and immersed in a solvent so as to dissolve the adhesive layer; making use of a vacuum device, the individual chips are then removed from the needle block and placed in chip carriers.

US-pat. 5,071,792 refers to a method of forming ultrathin integrated circuit chips. In a first step, grooves are produced in the front of the wafer. These grooves are then filled with a hard material acting as a grinding stop. This material is then planarized and a wax is applied thereto, which provides a temporary adhesion between a passivation coating and the planar surface of an intermediate support. Following this, the back of the wafer is ground so as to dice the chips. The comparatively hard material in the grooves acts here as a grinding stop. After the grinding process, the grinding stop material is removed from the grooves. In order to obtain the individual chips, the wax film is finally melted.

## Summary of the Invention

It is the object of the present invention to provide a reasonably-priced but still reliable method of dicing a wafer for obtaining very thin circuit chips.

In accordance with the present invention, this object is achieved by a method of dicing a wafer which comprises a plurality of circuit structures, said method comprising the steps of: defining a trench between at least two circuit structures on one face of the wafer; forming the trench down to a defined depth by means of dry etching; fixing to said one face of the wafer a re-

detachable intermediate support composed of a fixed intermediate support substrate and an adhesive medium which is applied to said intermediate support substrate and which can specifically be modified in terms of its adhesive strength and which can specifically be modified in terms of its adhesive strength, said adhesive medium being an adhesive foil which is adherent on both sides, the side of the adhesive foil which is secured to said one face of the wafer having the variable adhesive strength, and said adhesive strength being adapted to be reduced by heating or by applying ultra violet radiation; thinning the wafer by dry-etching, which is secured to the intermediate support, from the opposite face so as to obtain individual circuit chips which are held by the intermediate support; and removing the individual circuit chips from the intermediate support by heating said intermediate support or by applying ultra violet radiation to the adhesive foil so as to reduce the adhesive strength of said adhesive foil to such an extent that the circuit chips can be detached from the intermediate support.

The present invention is based on the finding that, for obtaining very thin circuit chips, mechanical effects must be eliminated as far as possible when the wafer is being diced. The danger that individual circuit chips may be damaged due to mechanical effects can be reduced markedly in this way. When very thin circuit chips are produced, it must be taken into account that the active region of a circuit chip may extend as deep as a few micrometers into the semiconductor material. When thin circuit chips having a thickness in the order of 20 µm are considered, only less than 20 µm will remain as a "support substrate" for the active region of the circuit chip. The present invention therefore departs from the concept of mechanical dicing, which is accomplished e.g. by scribing, sawing or breaking of thin

connections defined by trenches, as has been explained hereinbefore, an executes dicing by means of dry etching from the back.

According to the present invention, a wafer comprising a plurality of circuit structures is diced in such a way that a trench is first defined between at least two circuit structures. Subsequently, the trench is deepened down to a defined depth. Following this, a re-detachable intermediate support is fixed to the wafer face having the trench formed therein, whereupon the wafer is subjected to dry-etching from the opposite face until the trenches are exposed. In this way, a dicing process is achieved in the case of which the circuit chips have not been subjected to mechanical stresses.

When, in accordance with a specially preferred embodiment, also the trench is formed by dry-etching instead of being formed mechanically, the individual circuit chips will not be subjected to any mechanical stress at all during the whole wafer dicing process. This has the effect that also very thin circuit chips can be produced, without any marked increase in the reject rate.

According to a preferred embodiment, the wafer is pre-thinned by means of wet-chemical etching or grinding before the back is subjected to dry-etching, the pre-thinning with the aid of mechanical means being executed only to such an extent that it is almost impossible that the material which will finally form the circuit chips has already been impaired mechanically.

The component used as an intermediate support is preferably an adhesive foil which is adherent on both sides and one side of which adheres to a wafer substrate, whereas the other side thereof is connected to the wafer to be diced and has a variable adhesive strength so that, after the dry-etching step, the adhe-

sive strength of this side of the adhesive foil can be reduced to such an extent that the diced circuit chips can easily be detached for further processing, said reduction of the adhesive strength being caused by heating or by exposure to UV radiation.

Even if the trench is implemented by means of careful mechanical processing methods, it will already be possible to produce a plurality of circuit chips with a comparatively low reject rate due to the dry-etching from the back for the purpose of dicing the wafer. Such circuit chips can have a thickness which is less than 50 µm and which especially amounts to about 20 µm and can even be reduced down to 5 µm.

If, however, in accordance with the preferred course of action, also the trench is produced by dry-etching, i.e. without subjecting the material to excessive stress, a certain number of further advantages will be achieved insofar as the wafer areas which will finally define the thin circuit chips are not subjected to any mechanical stresses at all.

Due to the fact that the trench need not be particularly deep, since the chips are very thin, the formation of a trench in a process making use of a mask for etching is, in general, carried out in a comparatively short period of time so that, in comparison with sawing of a wafer, which may last several hours especially in the case of small chips and wafers having a diameter of 20 to 30 cm, a substantial increase in the throughput can be achieved. In addition, a substantially larger number of chips can - again in comparison with sawing - be accommodated on a wafer, especially in the case of small chips, since trenches produced by sawing normally have a thickness of approx. 100 µm, whereas only 10 µm will suffice for dry-etched trenches down to the aimed-at depth, which will correspond approximately to the

thickness of the circuit chips. In particular in the case of small chips, the number of chips per wafer can be increased by up to 10 to 15%.

Due to the fact that at least the back of the chips and, preferably, also the lateral edges thereof are subjected to an etch treatment, the chips are mechanically undamaged; this will be particularly important when the chips have to be bent, as will e.g. the case if the chips have to be incorporated in electronic labels.

Finally, arbitrary chip shapes can be produced especially by dry-etching the trench, i.e. the chip shapes that can be produced are not limited to rectangular shapes, as in the case of sawing; this can be of decisive importance especially in connection with power semiconductors, since chip corners, which would otherwise generate very high electric fields, can be eliminated. Finally, also the position of the chips can unequivocally be identified from the back, a circumstance which will be of great advantage e.g. for die bonding and for recognizing chips of good quality and those of poor quality.

## Brief Description of the Drawings

In the following, preferred embodiments of the present invention will be explained in detail making reference to the drawings enclosed, in which:

Fig. 1 shows a top view of a wafer which comprises a plurality of circuit chips and in which a trench is defined;

Fig. 2 shows a cross-sectional view of the wafer of Fig. 1 having the trench formed therein;

Fig. 3 shows a view of the wafer of Fig. 2 which is secured to an intermediate support;

Fig. 4 shows a view of the wafer of Fig. 3 after thinning of the wafer by means of a dry-etching process; and

Fig. 5 shows the individual circuit chips after their removal from the intermediate support.

## Detailed Description of Preferred Embodiments

Fig. 1 shows a top view of a detail of a wafer 10 comprising a plurality of fully processed individual circuit structures 12a, 12b. The wafer 10 has already defined thereon a trench 14. In cases in which the trench 14 is produced mechanically, the trench can be defined e.g. by inputting the coordinates for a sawing or scribing means. In cases in which the trench 14 is produced by making use of a dry-etching process, the trench is formed by applying a resist mask with side-wall protection by polymer deposition. Alternatively, the etch mask defining the trench 14 can also be implemented as an $SiO_2$ mask. Summarizing, it can be stated that all the methods of forming an etch mask can be used for defining the trench 14.

Fig. 2 shows a cross-sectional view along the line A-A of Fig. 1 through the wafer 10 in a state in which the trench 14 has been formed down to a certain depth d. The predetermined thickness is chosen such that it is at least equal to the target thickness of

the circuit chip to be produced so that the circuit chips can be diced later on without being mechanically acted upon.

If e.g. the process with polymer deposition is used, $SF_6$ can be used as an etching gas and $CHF_3$ and $C_2F_6$ can be used as polymer protection. More details with regard to this method are disclosed in DE 4241045.

If a process with an $SiO_2$ mask is used, a mixture of HBr, $Cl_2$, $O_2$ and He can be used as an etching gas. In addition, all the other known dry-etching processes can be used. Dry-etching in general has the substantial advantage that, in contrast to a mechanical implementation of the trench, the edges of the circuit chip are not subjected to mechanical stress and are therefore stable.

Fig. 3 shows the circuit chip 10, which is provided with the trench 14, after it has been secured to an intermediate support which can be composed of a substrate wafer 16a and an adhesive medium 16b. The medium used as an adhesive medium 16b is preferably an adhesive foil which is adherent on both sides, one side of this adhesive foil being provided with a special coating which loses its adhesive strength when it has been heated to a temperature of e.g. 90 to 140°. The other side does not have a varying adhesive strength. The support foil is attached in such a way that the side with the non-varying adhesive strength is connected to the wafer support 16a, whereas the side with the varying adhesive strength is connected to the semiconductor wafer 10, as can be seen in Fig. 3. An essential property of the intermediate support 16a, 16b is that the adhesive connection with the wafer 10 can be released. In addition, a full-area, cavity-free connection will be of advantage.

Alternative materials for the adhesive medium 16b are thermoplastic materials or adhesive foils whose adhesive strength can be varied not by means of heat but by means of UV light. If UV-sensitive foils are used, the support substrate 16a must be transparent. In this case, a glass wafer can be used as a support substrate.

When the wafer 10 has been glued onto the intermediate support 16a, 16b, the wafer is thinned from the back, as shown in Fig. 4. If the initial wafer 10 is already comparatively thin, it will presumably suffice to use only a dry-etching process so as to separate the individual circuit chips from one another, i.e. so as to remove the back at least up to the trench. If the wafer in question is, however, a thick wafer, e.g. a wafer having a thickness of 700 µm, which is a typical value for commercially available wafers, a faster method, such as mechanical grinding, wet etching or the like, is preferably used prior to the final dry-etching step for dicing the circuit chips. A method which proved to be advantageous is the so-called spin-etching in the case of which the wafer lies on a rotating disk while the etching medium flows onto the disk from above and is spun off therefrom.

When the wafer has been pre-thinned to a predetermined thickness, the last step of dicing is left to the dry-etching process. The etching gases preferably used for executing this step are the etching gas mixture $Cl_2$ and $CF_4$, or $SF_6$ as a single etching gas. It should here be noted that a chemical treatment with chlorine and fluorine is generally well suited for etching silicon. The etching gas $NF_3$ is very efficient as well, but, at present, it is still comparatively expensive; hence, it is one of the less preferred etching gases at the present time.

As can be seen in Fig. 4, individual circuit chips 18, 20, 22 and 24 have now been created, which are no longer connected to one another but which are only held by the adhesive medium 16b. In cases in which an adhesive foil is used which is adherent on both sides and which has a variable adhesive strength on one side thereof, the individual circuit chips 18, 20, 22, 24 can now easily be removed by varying the adhesive strength so that they will then exist completely independently of one another, as can be seen in Fig. 5, whereupon they are picked up by an assembly machine or a similar device so as to be accommodated at their final location.

It should here be pointed out that this method is suitable not only for silicon wafers but also for GaAs wafers, which are particularly sensitive to mechanical stress due to their brittleness, as well as for other III-V semiconductors. It goes without saying that for semiconductor materials other than silicon etching gases other than the above-mentioned ones are also used.

The diced thin circuit chips 18, 20, 22, 24 can be used in electronic components and systems requiring an extremely small volume demand, e.g. in mobile telecommunications systems or medical monitoring and assistance systems, such as hearing aids, cardiac pacemakers, monitoring and diagnostic units worn on the body, etc..

Other fields of use are electronic components which are optimized for electric signal transmission, such as high-frequency components.

Finally, the thin circuit chips diced according to the present invention can be combined so as to obtain circuit modules which comprise individual components consisting of different basic ma-

terials or in which chips originating from different manufacturing technologies are joined. Ultrathin circuit chips can be used especially in systems consisting of memory chips, logic chips, sensor components, chip-card chips, power components or high-frequency transmission chips (transponders).

Due to their very small thickness, thin circuit chips produced according to the present invention contribute to the overall volume of the component only as a thin film. A complete chip system consisting e.g. of a normal chip and an ultrathin chip is, in the final analysis, not much larger than a standard integrated circuit.

Due to the small thickness of the diced circuit chips, it is now also possible to use surface treatment techniques for contacting and wiring individual chips in a multi-chip module making use of conventional techniques which require planar or almost planar surfaces.

Finally, the method according to the present invention can be used for dicing not only specially produced or pretreated circuit wafers but all wafers which can be obtained from arbitrary manufacturers as fully processed wafers.

Claims

1. A method of dicing a wafer which comprises a plurality of circuit structures, said method comprising the steps of:

defining a trench between at least two circuit structures on one face of the wafer;

forming the trench down to a defined depth by means of dry etching;

fixing to said one face of the wafer a re-detachable intermediate support composed of a fixed intermediate support substrate and an adhesive medium which is applied to said intermediate support substrate and which can specifically be modified in terms of its adhesive strength and which can specifically be modified in terms of its adhesive strength, said adhesive medium being an adhesive foil which is adherent on both sides, the side of the adhesive foil which is secured to said one face of the wafer having the variable adhesive strength, and said adhesive strength being adapted to be reduced by heating or by applying ultra violet radiation;

thinning the wafer by dry-etching, which is secured to the intermediate support, from the opposite face so as to obtain individual circuit chips which are held by the intermediate support; and

removing the individual circuit chips from the intermediate support by heating said intermediate support or by applying ultra violet radiation to the adhesive foil so as to reduce

the adhesive strength of said adhesive foil to such an extent that the circuit chips can be detached from the intermediate support.

2. A method according to claim 1, wherein the dry-etching step of the other face of the wafer is executed until the circuit chips have a thickness which is smaller than 50 µm and which is preferably 20 µm.

3. A method according to claim 1,

wherein the forming of the trench is carried out such that a predetermined thickness is reached, which corresponds to a target chip thickness; and

wherein the step of dry- etching the other face of the wafer is executed until the trench has substantially been reached.

4. A method according to claim 1,

wherein, prior to the step of dry etching the other face of the wafer, a pre-thinning step is executed in such a way that the circuit chips are still interconnected across the trench and that the thickness of this connection has a specific value.

5. A method according to claim 4, wherein the pre-thinning step comprises grinding, wet-chemical etching or a combination thereof.

6. A method according to claim 1, wherein in the trench-defining step a trench having at least one round portion is

defined.

7. A method according to claim 1, wherein the wafer consists of Si, GaAs or some other III-V semiconductor.

8. A method according to claim 1, wherein the defining step comprises the application of an $SiO_2$ mask or of a resist mask with side-wall protection by polymer deposition.

**Method of Subdividing a Wafer**

Abstract

In a method of dicing a wafer, which comprises a plurality of individual circuit structures, a trench is first defined between at least two circuit structures on one face of the wafer. Subsequently, the trench is deepened down to a defined depth. Following this, one face of the wafer has fixed thereto a re-detachable intermediate support composed of a fixed intermediate support substrate and an adhesive medium which is applied to said intermediate support substrate and which can specifically be modified in terms of its adhesive strength, whereupon the wafer is dry-etched from the opposite face so that circuit chips are obtained which are connected to one another only via the intermediate support. Subsequently, the circuit chips are removed from the intermediate support. This method substantially reduces mechanical impairments that may occur during dicing of the circuit chips; on the one hand, this permits the production of circuit chips with a thickness of less than 50 µm and, on the other hand, it leads to mechanically substantially undamaged circuit chips.

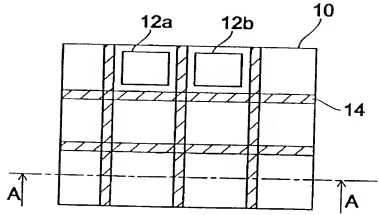


Fig. 1

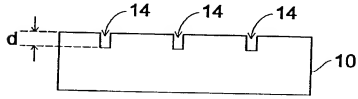


Fig. 2

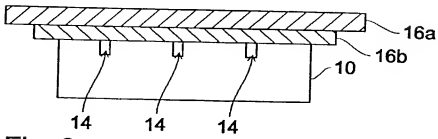


Fig. 3

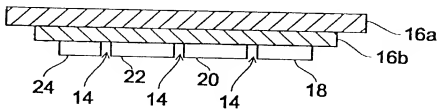


Fig. 4

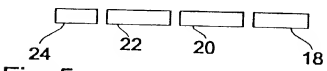


Fig. 5

**Practitioner's Docket No.** _____ *PATENT*

## COMBINED DECLARATION AND POWER OF ATTORNEY

## (ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION, OR C-I-P)

As a below named inventor, I hereby declare that:

### TYPE OF DECLARATION

This declaration is for a national stage of PCT application.

### INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

### TITLE OF INVENTION

Method of Subdividing a Wafer

### SPECIFICATION IDENTIFICATION

The specification was described and claimed in PCT International Application No. PCT/EP00/05772 filed on June 21, 2000.

### ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, Section 1.56, and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent.

### PRIORITY CLAIM (35 U.S.C. Section 119(a)-(d))

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

Such applications have been filed as follows.

**PRIOR PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. SECTION 119(a)-(d)**

| INDICATE IF PCT | APPLICATION NUMBER | DATE OF FILING DAY, MONTH, YEAR | PRIORITY CLAIMED UNDER 35 U.S.C. SECTION 119 |
|---|---|---|---|
| PCT | PCT/EP00/05772 | 21/June/2000 | yes |

**PRIOR FOREIGN APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. SECTION 119(a)-(d)**

| COUNTRY | APPLICATION NUMBER | DATE OF FILING DAY, MONTH, YEAR | PRIORITY CLAIMED UNDER 35 U.S.C. SECTION 119 |
|---|---|---|---|
| European | 99 112 540.2 | 01/July/1999 | yes |
| Germany | 199 62 763.0 | 23/December/1999 | yes |

**POWER OF ATTORNEY**

I hereby,appoint the practitioner(s) associated with the Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

**Customer No. 24283**

SEND CORRESPONDENCE TO
**Customer No. 24283**

DIRECT TELEPHONE CALLS TO:
Carl A. Forest
303-379-1114

**DECLARATION**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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